# Series IP440A Industrial I/O Pack
# 32-Channel Isolated Digital Input Module
# With Interrupts

# USER'S MANUAL


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**IMPORTANT SAFETY CONSIDERATIONS**

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

## 1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP440A module provides 32 channels of isolated digital inputs for interfacing to the VMEbus or PCI bus, according to your carrier board. Four units may be mounted on a single carrier board to provide up to 128 inputs per system slot. Inputs of this module are bipolar and can be used to sense positive or negative voltages in 3 ranges according to the model:

| MODEL | INPUT RANGE | THRESHOLD |
|---|---|---|
| IP440A-1 | ± 4V to ±18V DC or AC peak | ± 4V Max |
| IP440A-2 | ± 16 to ±40V DC or AC peak | ± 16V Max |
| IP440A-3 | ± 38 to ±60V DC or AC peak | ± 38V Max |

| MODEL | OPERATING TEMPERATURE RANGE |
|---|---|
| IP440A-X | 0 to +70°C |
| IP440A-XE | -40 to +85°C |

The inputs normally function as independent input level detectors without interrupts. However, each input line includes built-in event sense circuitry with programmable polarity, debounce, and interrupt support. Inputs also include hysteresis for increased noise immunity. The IP440A utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial I/O applications that require a high-density, highly reliable, high-performance interface at a low cost.

### KEY IP440A FEATURES

- **High Channel Count** - Provides programmable monitor and control of 32 optically isolated input points. Four units mounted on a carrier board provide 128 isolated input points in a single VMEbus or PCI system slot.
- **High-Speed/0 Wait States** - No wait states are required for all read/write cycles (all cycles complete in 250ns) and hold states are supported.
- **Wide Range Bipolar Input Voltage** - Three model ranges provide interface capability for bipolar voltages from ±4 to ±60V DC or AC peak (see Specifications section).
- **Optically Isolated** - Individual bipolar opto-couplers provide isolation. There are four groups (ports) of 8 channels, each which include separate port commons to ensure port-to-port isolation. Individual ports are isolated from each other and from the logic.
- **Programmable Polarity Event Interrupts** - Interrupts are software programmable for positive (low-to-high) or negative (high-to-low) input level transitions on all 32 channels. Using two channels per input, change-of-state transitions may also be configured.
- **Input Hysteresis** - Isolated inputs include hysteresis for increased noise immunity.
- **Programmable Debounce** - The event sense input circuitry includes programmable debounce times for all 32 channels. Debounce time is the duration of time that must pass before

the input transition is recognized as valid at the FPGA input. This helps prevent false events and increases noise immunity.

- **Reverse Polarity Protection** - Bipolar inputs are not polarized and are inherently reverse polarity protected.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set.
- **Loopback Compatible with IP445 Output Module** - The field side P2 pinouts of this model are directly compatible with those of the Acromag Model IP445 32-Channel Digital Output Module for direct closed-loop monitoring of the output states. The IP440A also shares the same P2 pinout used on the Acromag non-isolated IP400 40 Channel Input Module, IP405 40-Channel Output Module, and IP408 32-Channel I/O Module, for channels 0-31. Likewise, this model may interface with industry standard I/O panels, termination panels, and relay racks when used with an Acromag Model 5025-655 I/O Adaptor Card. However, since relay racks generally provide isolation, it may be more efficient to interface with them using the non-isolated IP400 input module.

**INDUSTRIAL I/O PACK INTERFACE FEATURES**

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 128 isolated input points in a single system slot. Both VMEbus and PCI bus carriers are supported.
- **Local ID** - Each IP module has its own 8-bit ID PROM which is accessed via data transfers in the "ID Read" space.
- **8-bit I/O** - Port register Read/Write is performed through 8-bit data transfer cycles in the IP module I/O space.
- **High Speed with No Wait States** - Access times for all data transfer cycles are described in terms of "wait" states--0 wait states are required for all read and write operations of this model. See Specifications section for detailed information.

**SIGNAL INTERFACE PRODUCTS**

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board. Acromag's AVME9630/9668 3U/6U non-intelligent VMEbus carrier boards and Acromag's APC8620 series PCI bus carrier boards are supported. A wide range of other Acromag IP modules are available to serve your signal conditioning and interface needs.

**Cables:**

Model 5025-551-X (Shielded Cable) or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting to the AVME9630/9660, other compatible carrier boards, or Model 5025-552 termination panels. The shielded cable is recommended for optimum performance with precision analog I/O applications, while the unshielded cable is recommended for digital I/O. The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request.

**Termination Panel:**

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

**Transition Module:**

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from the card cage. It is available for use in card cages, which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to AVME9630/9660 boards via a flat 50-pin ribbon cable within the card cage (cable Model 5025-550-X or 5025-551-X).

**IP MODULE Win32 DRIVER SOFTWARE**

Acromag provides a software product (sold separately) to facilitate the development of Windows (98/Me/2000/XP®) applications accessing Industry Pack modules installed on Acromag PCI Carrier Cards and CompactPCI Carrier Cards. This software (Model IPSW-API-WIN) consists of low-level drivers and Windows 32 Dynamic Link Libraries (DLLS) that are compatible with a number of programming environments including Visual C++, Visual Basic, Borland C++ Builder and others. The DLL functions provide a high-level interface to the carriers and IP modules eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers.

**IP MODULE VXWorks SOFTWARE**

Acromag provides a software product (sold separately) consisting of board VxWorks® software. This software (Model IPSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, ACPC8630/35, and ACPC8625. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PCI boards.

**IP MODULE QNX SOFTWARE**

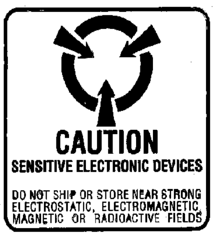
Acromag provides a software product (sold separately) consisting of board QNX® software. This software (Model IPSW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8620A/21A, ACPC8630/35, and ACPC8625. The software supports X86 PCI bus only and is implemented as library of "C" functions. These functions link with existing user code to make possible simple control of all Acromag IP modules and carriers.

## 2.0 PREPARATION FOR USE

### UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.




This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

### CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

> **IMPORTANT:** Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

### BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Model IP440A digital input boards have no hardware jumpers or switches to configure.

### CONNECTORS

**IP Field I/O Connector (P2)**

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) that mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

**Table 2.1: IP440A Field I/O Pin Connections (P2)**

| Pin Description | | Number | Pin Description | | Number |
|---|---|---|---|---|---|
| **PORT 0** | IN00 | 1 | **PORT 2** | IN16 | 21 |
| | IN01 | 2 | | IN17 | 22 |
| | IN02 | 3 | | IN18 | 23 |
| | IN03 | 4 | | IN19 | 24 |
| | NC | 5 | | NC | 25 |
| | IN04 | 6 | | IN20 | 26 |
| | IN05 | 7 | | IN21 | 27 |
| | IN06 | 8 | | IN22 | 28 |
| | IN07 | 9 | | IN23 | 29 |
| | ACOM | 10 | | CCOM | 30 |
| **PORT 1** | IN08 | 11 | **PORT 3** | IN24 | 31 |
| | IN09 | 12 | | IN25 | 32 |
| | IN10 | 13 | | IN26 | 33 |
| | IN11 | 14 | | IN27 | 34 |
| | NC | 15 | | NC | 35 |
| | IN12 | 16 | | IN28 | 36 |
| | IN13 | 17 | | IN29 | 37 |
| | IN14 | 18 | | IN30 | 38 |
| | IN15 | 19 | | IN31 | 39 |
| | BCOM | 20 | | DCOM | 40 |
| | | | | No Connection | 41 |
| | | | | No Connection | 42 |
| | | | | No Connection | 43 |
| | | | | No Connection | 44 |
| | | | | No Connection | 45 |
| | | | | No Connection | 46 |
| | | | | No Connection | 47 |
| | | | | No Connection | 48 |
| | | | | No Connection | 49 |
| | | | | No Connection | 50 |

Input channels of this module are divided into four ports of eight channels each. Channels of a port share a common signal connection with each other. Isolation is provided between ports and between each port and the IP logic. With respect to interrupt generation and events, event polarities may be defined as positive (low-to-high), or negative (high-to-low) for individual nibbles (groups of 4 input lines, or half ports). Change-of-State detection would require 2 input channels--one detecting positive events, one detecting negative events.

P2 pinouts are arranged to be compatible with similar industry models. This model is directly loopback compatible with the Acromag Model IP445 Digital Output Module. Likewise, pin assignments are identical to those of Acromag Model IP400 40-Channel Digital Input Boards for channels 0-31. This model may also interface with industry accepted I/O panels, termination panels, and relay racks when used with the Acromag Model 5025-655 I/O Adapter Card. Consult the factory for information on these and other compatible products.

See Drawing 4502-048 for loopback connections to Acromag Model IP445 Output Modules. Drawing 4502-048 also gives an example of how to interface the IP440A-1 with open-drain TTL outputs signals.

Note that the inputs of this device are bipolar, and may be connected in any direction with respect to the port common. Further, do not confuse port commons with signal ground. For the IP440A, port common only infers that this lead is connected common to the 8 inputs of the port (a separate port common for each port). Likewise, the port commons of the IP440A input module and IP445 output module are normally not connected together for loopback interconnection (see Drawing 4502-048).

**Noise and Grounding Considerations**

Input lines of the IP440A are optically isolated between the logic and field input connections. Likewise, separate port commons facilitate port-to-port isolation. Consequently, the field I/O connections are isolated from the carrier board and backplane, thus minimizing the negative effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations to avoid inadvertent isolation bridges, noise pickup, isolation voltage clearance violations, equipment failure, or ground loops.

**IP Logic Interface Connector (P1)**

P1 of the IP module provides the logic interface to the mating connector on the carrier board. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold plating in the mating area.

Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

**Table 2.2: Standard Logic Interface Connections (P1)**

| Pin Description | Number | Pin Description | Number |
|---|---|---|---|
| GND | 1 | GND | 26 |
| CLK | 2 | +5V | 27 |
| Reset* | 3 | R/W* | 28 |
| D00 | 4 | IDSEL* | 29 |
| D01 | 5 | ***DMAReq0**** | 30 |
| D02 | 6 | MEMSEL* | 31 |
| D03 | 7 | ***DMAReq1**** | 32 |
| D04 | 8 | IntSel* | 33 |
| D05 | 9 | ***DMAck0**** | 34 |
| D06 | 10 | IOSEL* | 35 |
| D07 | 11 | ***RESERVED*** | 36 |
| ***D08*** | 12 | A1 | 37 |
| ***D09*** | 13 | ***DMAEnd**** | 38 |
| ***D10*** | 14 | A2 | 39 |
| ***D11*** | 15 | ***ERROR**** | 40 |
| ***D12*** | 16 | A3 | 41 |
| ***D13*** | 17 | INTReq0* | 42 |
| ***D14*** | 18 | A4 | 43 |
| ***D15*** | 19 | ***INTReq1**** | 44 |
| BS0* | 20 | A5 | 45 |
| ***BS1**** | 21 | ***STROBE**** | 46 |
| ***-12V*** | 22 | A6 | 47 |
| ***+12V*** | 23 | ACK* | 48 |
| +5V | 24 | ***RESERVED*** | 49 |
| GND | 25 | GND | 50 |

An Asterisk (*) is used to indicate an active-low signal.
***BOLD ITALIC*** Logic Lines are NOT USED by this IP Model.

## 3.0 PROGRAMMING INFORMATION

**ADDRESS MAPS**

This board is addressable in the Industrial Pack I/O space to control the configuration and status monitoring of 32 digital input or event channels.

This board operates in two modes: Standard Mode and Enhanced Mode. Standard Mode provides digital input voltage monitoring of 32 isolated signal lines. In Standard Mode, each input line is configured as a simple input without interrupts. Data is read from (or written to) one of eight groups (ports) as designated by the address and read and write signals. Enhanced Mode includes the same functionality of Standard Mode, but adds access to 32 additional event sense inputs connected to each input point of ports 0-3. Individual inputs also include selectable hardware debounce in Enhanced Mode. For event sensing, the Enhanced Mode allows a specific input level transition (High-to-Low, Low-to-High, or Change-of-State) to be detected and optionally generate an interrupt.

Memory is organized and addressed in separate banks of eight registers or ports (eight ports to a bank). The Standard Mode of operation addresses the first group of 8 registers or ports (ports 0-3 for reading inputs, Ports 4, 5, & 6 which are not used on this model, and Port 7 which is the Mask Register). If the Enhanced Mode is selected, then 3 additional banks of 8 registers are accessed to cover the additional functionality in this mode (events, interrupts, and debounce). The first bank of the Enhanced Mode (bank 0) is similar in operation to the Standard

Mode. The second bank (bank 1) provides event sense and interrupt control. The third bank is used to configure the debounce circuitry to be applied to input channels in the Enhanced Mode. Two additional mode-independent registers are provided to enable the interrupt request line, generate a software reset, and store the interrupt vector.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP440A uses only a portion of this space. The I/O space address map for the IP440A is shown in Table 3.1. Note the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. All accesses are performed on an 8-bit byte basis (D0..D7).

This manual is presented using the “Big Endian” byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or “Little Endian” byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on a PCI carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier will require the use of odd address locations.

Note that some functions share the same register address. For these items, the address lines are used along with the read and write signals to determine the function required.

**Standard (Default) Mode Memory Map**

Table 3.1A shows the memory map for the Standard Mode of operation. This is the Default mode reached after power-up or system reset. Standard Mode provides simple monitoring of 32 digital input lines without interrupts. Data is read from or written to one of eight groups (ports) as designated by the address and read and write signals.

To switch to Enhanced Mode, four unique bytes must be written to port 7, in consecutive order, without doing any reads or writes to any other port and with interrupts disabled. The data pattern to be written is 07H, 0DH, 06H, and 12H, and this must be written after reset or power-up.

**Enhanced Mode Memory Maps**

Table 3.1B shows the memory maps used for the Enhanced Mode of operation. Enhanced Mode includes the same functionality of Standard Mode, but allows each input port’s event sense input and debounce logic to be enabled.

In Enhanced Mode, a memory map is given for each of 3 memory banks. The first memory bank (bank 0) has the same functionality as the Standard Mode. Additionally, its port 7 register is used to select which bank to access (similar to Standard Mode where port 7 was used to select the Enhanced Mode). Bank 1 provides read/write access to the 32 event sense inputs. Bank 2 provides access to the registers used to control the debounce circuitry of these event sense inputs.

**Table 3.1A: IP440A R/W Space Address (Hex) Memory Map**

| EVEN Base Addr+ | MSB D15 D08 | LSB D07 D00 | ODD Base Addr+ |
|---|---|---|---|
| **STANDARD MODE (DEFAULT) REGISTER DEFINITIONS:** | | | |
| **00** | Not Driven[4] | READ[1] - Port 0 Register IN00-IN07 | **01** |
| **02** | Not Driven[4] | READ[1] - Port 1 Register IN08-IN/15 | **03** |
| **04** | Not Driven[4] | READ[1] - Port 2 Register IN16-IN23 | **05** |
| **06** | Not Driven[4] | READ[1] - Port 3 Register IN24-IN31 | **07** |
| **08** | Not Driven[4] | READ/WRITE - Port 4 NOT USED[2] | **09** |
| **0A** | Not Driven[4] | READ/WRITE - Port 5 NOT USED[2] | **0B** |
| **0C** | Not Driven[4] | READ/WRITE - Port 6 NOT USED[2] | **0D** |
| **0E** | Not Driven[4] | READ/WRITE - Port 7 WRITE MASK REGISTER AND ENHANCED MODE SELECT REGISTER[3] | **0F** |
| **10 ↓ 7E** | NOT USED[2] | | **11 ↓ 7F** |

**Notes (Table 3.1A):**

1. Writes to these registers may have an adverse effect on module operation. Use the Port 7 Write Mask to prevent writing to these registers.
2. The IP will respond to addresses that are “Not Used” with an active IP module acknowledge (ACK*). The board will return “0” for all address reads that are not used or reserved.
3. Writing four unique bytes (07H, 0DH, 06H, and 12H) to port 7, in consecutive order, will switch to Enhanced Mode. Perform this operation after reset or power-up with interrupts disabled. Do not read or write to any other port between writes.
4. The upper 8 bits of these registers are not driven and pull-ups on the carrier data bus will cause these bits to read high (1’s).

**Table 3.1B: IP440A R/W Space Address (Hex) Memory Map**

| EVEN Base Addr+ | MSB D15 D08 | LSB D07 D00 | ODD Base Addr+ |
|---|---|---|---|
| **ENHANCED MODE, REGISTER BANK [0] DEFINITIONS:** | | | |
| **00** | Not Driven[1] | READ[4] - Port 0 Register IN00-IN07 | **01** |
| **02** | Not Driven[1] | READ[4] -Port 1 Register IN08-IN15 | **03** |
| **04** | Not Driven[1] | READ[4] - Port 2 Register IN16-IN23 | **05** |
| **06** | Not Driven[1] | READ[4] - Port 3 Register IN24-IN31 | **07** |
| **08** | Not Driven[1] | READ[2] - Port 4 NOT USED | **09** |
| **0A** | Not Driven[1] | READ[2] - Port 5 NOT USED | **0B** |
| **0C** | Not Driven[1] | READ[2] - Port 6 NOT USED | **0D** |
| **0E** | Not Driven[1] | READ - Port 7 READ MASK REGISTER (Also Current Bank Status) | **0F** |
| **0E** | Not Driven[1] | WRITE - Port 7 WRITE MASK REGISTER (Also Bank Select Register) | **0F** |

**Table 3.1B: IP440A R/W Space Address (Hex) Memory Map**

| EVEN Base Addr+ | MSB D15 D08 | LSB D07 D00 | ODD Base Addr+ |
|---|---|---|---|
| **ENHANCED MODE, REGISTER BANK [1] DEFINITIONS:** | | | |
| 00 | Not Driven[1] | READ - Port 0 Event Sense Status Reg. (Port 0 Input points 0-7) | 01 |
| 00 | Not Driven[1] | WRITE - Port 0 Event Sense Clear Reg (Port 0 Input points 0-7) | 01 |
| 02 | Not Driven[1] | READ - Port 1 Event Sense Status Reg. (Port 1 Input points 8-15) | 03 |
| 02 | Not Driven[1] | WRITE - Port 1 Event Sense Clear Reg (Port 1 Input points 8-15) | 03 |
| 04 | Not Driven[1] | READ - Port 2 Event Sense Status Reg. (Port 2 Input points 16-23) | 05 |
| 04 | Not Driven[1] | WRITE - Port 2 Event Sense Clear Reg (Port 2 Input points 16-23) | 05 |
| 06 | Not Driven[1] | READ - Port 3 Event Sense Status Reg. (Port 3 Input points 24-31) | 07 |
| 06 | Not Driven[1] | WRITE - Port 3 Event Sense Clear Reg (Port 3 Input points 24-31) | 07 |
| 08 | Not Driven[1] | READ - Port 4 NOT USED[2] | 09 |
| 08 | Not Driven[1] | WRITE - Port 4 NOT USED[2] | 09 |
| 0A | Not Driven[1] | READ - Port 5 NOT USED[2] | 0B |
| 0A | Not Driven[1] | WRITE - Port 5 NOT USED[2] | 0B |
| 0C | Not Driven[1] | READ - Port 6 Event Status for Ports 0-3 and Interrupt Status Reg. | 0D |
| 0C | Not Driven[1] | WRITE - Port 6 Event Polarity Control Register for Port 0-3 | 0D |
| 0E | Not Driven[1] | READ - Port 7 Current Bank Status Reg. | 0F |
| 0E | Not Driven[1] | WRITE - Port 7 Bank Select Register | 0F |
| **ENHANCED MODE, REGISTER BANK [2] DEFINITIONS:** | | | |
| 00 | Not Driven[1] | READ/WRITE - Port 0 Debounce Control Register (for Ports 0-3) | 01 |
| 02 | Not Driven[1] | READ/WRITE - Port 1 Debounce Duration Reg. 0 (for Ports 0-3) | 03 |
| 04 | Not Driven[1] | NOT USED | 05 |
| 06 | Not Driven[1] | WRITE ONLY - Port 3 Debounce Clock Select | 07 |
| 08 ↓ 0C | Not Driven[1] | Port 4,5,6 NOT USED[2] | 09 ↓ 0D |
| 0E | Not Driven[1] | READ/WRITE - Port 7 Bank Status/Select Register | 0F |

**Table 3.1B: IP440A R/W Space Address (Hex) Memory Map**

| EVEN Base Addr+ | MSB D15 D08 | LSB D07 D00 | ODD Base Addr+ |
|---|---|---|---|
| **INDEPENDENT FIXED FUNCTION REGISTERS:** | | | |
| 10 ↓ 1C | Not Driven[1] | NOT USED[2] | 11 ↓ 1D |
| 1E | Not Driven[1] | READ/WRITE Interrupt Enable Register (Bit 0=1 enables INTREQ0) & Software Reset Generator (Bit 1=1 Generates Reset) | 1F |
| 20 ↓ 2C | Not Driven[1] | NOT USED[2] | 21 ↓ 2D |
| 2E | Not Driven[1] | READ/WRITE Interrupt Vector Register | 2F |
| 30 ↓ 7E | Not Driven[1] | NOT USED[2] | 31 ↓ 7F |

**Notes (Table 3.1B):**

1. The upper 8 bits of these registers are not driven and pull-ups on the carrier data bus will cause these bits to read high (1's).
2. The IP will respond to addresses that are "Not Used" with an active IP module acknowledge (ACK*). The board will return "0" for all address reads that are not used or reserved.
3. All Reads and Writes are 0 wait state.
4. Writes to these registers may have an adverse effect on module operation. Use the Port 7 Write Mask to prevent writing to these registers.

**REGISTER DEFINITIONS**

**STANDARD MODE REGISTERS**

**Port Registers**
**(Standard Mode, Ports 0-3, Read Only)**

Four registers are provided to monitor 32 possible input points. Data is read from one of four groups of eight input lines (Ports 0-3), as designated by the address and read and write signals. Each port assigns the least significant data line (D0) to the least significant input line of the port grouping (e.g. IN00 for port 0 to D0). A read of this register returns the status (ON/OFF) of the input point. ***Do not write to these registers.*** The Mask Register is used to disable writes to these ports. On power-up or reset, the ports are reset to 0.

**Write Mask Register & Enhanced Mode Select Register**
**(Standard Mode, Port 7, Read/Write)**

This register is used to mask the ability to write data to the four I/O ports of this model. Writing a '1' to bits 0-3 of the Mask Register will mask ports 0-3 respectively, from inadvertent writes. A read of this register will return the status of the mask in bits 0-3.

**Standard Mode Write Mask Register (Port 7)**

| BIT | WRITE TO REGISTER | READ FROM REGISTER |
|---|---|---|
| 0 | Port 0 Write Mask | Port 0 Write Mask |
| 1 | Port 1 Write Mask | Port 1 Write Mask |
| 2 | Port 2 Write Mask | Port 2 Write Mask |
| 3 | Port 3 Write Mask | Port 3 Write Mask |
| 4-7 | NOT USED | NOT USED |

Bits 4-7 of this register are not used. On power-up reset, all bits are set to ‘0’.

To switch to Enhanced Mode, four unique bytes must be written to port 7, in consecutive order, without doing any reads or writes to any other port and with interrupts disabled. The data pattern to be written is 07H, 0DH, 06H, and 12H, in order, and this must be written immediately after reset or power-up.

## ENHANCED MODE

### BANK 0 REGISTERS

**Port Registers**
**(Enhanced Mode Bank 0, Ports 0-3, Read Only)**

Four input registers are provided to monitor 32 possible input points. Data is read from one of four groups (Ports 0-3) of eight input lines, as designated by the address. Each port assigns the least significant data line (D0) to the least significant input line of the port grouping (e.g. IN00 of port 0 to D0). A read of this register returns the status (ON/OFF) of the input signal. ***Do not write to these registers.*** The Mask Register is used to disable writes to these ports.

**Write Mask Register and Bank Select Register 0**
**(Enhanced Mode Bank 0, Port 7, Read/Write)**

This register is used to mask the ability to write data to the four I/O ports of this model. Writing a ‘1’ to bits 0-3 of the Mask Register will mask ports 0-3 respectively, from inadvertent writes. A read of this register will return the status of the mask in bits 0-3.

**Enhanced Mode Write Mask Register (Port 7)**

| BIT | WRITE TO REGISTER | READ FROM REGISTER |
|---|---|---|
| 0 | Port 0 Write Mask | Port 0 Write Mask |
| 1 | Port 1 Write Mask | Port 1 Write Mask |
| 2 | Port 2 Write Mask | Port 2 Write Mask |
| 3 | Port 3 Write Mask | Port 3 Write Mask |
| 4-5 | NOT USED | NOT USED |
| 6 | Bank Select Bit 0 | Bank Status Bit 0 |
| 7 | Bank Select Bit 1 | Bank Status Bit 1 |

Bits 6 & 7 of this register are used to select/monitor the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0-2) of eight registers may be addressed. Bank 0 registers are similar to the Standard Mode bank of registers. Bank 1 allows the 32 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of the event inputs. Bits 7 and 6 select the bank as follows:

**Enhanced Mode Bank Select**

| Bit 7 Bit 6 | BANK OF REGISTERS |
|---|---|
| 00 | Bank 0 - Read Input Signals |
| 01 | Bank 1 - Event Status/Clear |
| 10 | Bank 2 - Event Debounce Control, Clock, and Duration |
| 11 | INVALID - DO NOT WRITE |

On power-up reset, this device is placed into Standard Mode and all bits are set to “0”.

### BANK 1 REGISTERS

**Event Sense Status & Clear Registers For IN00-IN31**
**(Enhanced Mode Bank 1, Ports 0-3, Read/Write)**

Each input line of each port includes an event sense input. Reading each port will return the status of each input port’s sense lines. Writing ‘0’ to a bit position of each port will clear the event on the corresponding line. When writing ports 0-3 of Enhanced Mode bank 1, each data bit written with logic 0 clears the corresponding event sense flip/flop. Further, each data bit of ports 0-3 must be written with a 1 to re-enable the corresponding event sense input after it is cleared. Reading ports 0-3 of the Enhanced Mode bank 1 returns the current event sense flip/flop status.

**Port 0 Event Sense/Status Register (Ports 1-3 are Similar)**

| BIT | READ PORT | WRITE “0” | WRITE “1” |
|---|---|---|---|
| 0 | Port 0 IN00 Event Status | Clear IN00 Event Sense Flip/Flop | Re-enable IN00 Event Sense |
| 1 | Port 0 IN01 Event Status | Clear IN01 Event Sense Flip/Flop | Re-enable IN01 Event Sense |
| 2 | Port 0 IN02 Event Status | Clear IN02 Event Sense Flip/Flop | Re-enable IN02 Event Sense |
| 3 | Port 0 IN03 Event Status | Clear IN03 Event Sense Flip/Flop | Re-enable IN03 Event Sense |
| 4 | Port 0 IN04 Event Status | Clear IN04 Event Sense Flip/Flop | Re-enable IN04 Event Sense |
| 5 | Port 0 IN05 Event Status | Clear IN05 Event Sense Flip/Flop | Re-enable IN05 Event Sense |
| 6 | Port 0 IN06 Event Status | Clear IN06 Event Sense Flip/Flop | Re-enable IN06 Event Sense |
| 7 | Port 0 IN07 Event Status | Clear IN07 Event Sense Flip/Flop | Re-enable IN07 Event Sense |

**Event Interrupt Status Register for Ports 0-3**
**(Enhanced Mode Bank 1, Port 6, Read Only)**

Reading this register will return the event interrupt status of input ports 0-3 (bits 0-3) and the interrupt status flag (bit 7). Bit 7 of this register indicates an event sense was detected on any of the 4 event sense ports (“1” = interrupt asserted/event sensed). Note that the interrupt status flag may optionally drive the Interrupt Request Line of the carrier board (see Interrupt Enable Register).

**Event Interrupt Status Register for Ports 0-3**

| BIT | READ EVENT STATUS REGISTER |
|---|---|
| 0 | Port 0 Interrupt Status (IN00-IN07) |
| 1 | Port 1 Interrupt Status (IN08-IN15) |
| 2 | Port 2 Interrupt Status (IN16-IN23) |
| 3 | Port 3 Interrupt Status (IN24-IN31) |
| 4-6 | NOT USED |
| 7 | Interrupt Status Flag |

**Event Polarity Control Register For Ports 0-3**
**(Enhanced Mode Bank 1, Port 6, Write Only)**

A write to this register controls the polarity of the input sense event for nibbles of ports 0-3 (channels 0-31, four channels at a time). A "1" written to a bit in this register will cause the corresponding event sense input lines to flag negative events (high-to-low transitions). A "0" will cause positive events to be sensed (low-to-high transitions). The polarity of the event sense logic must be set prior to enabling the event input logic. Note that no events will be detected until enabled via the Event Sense Status & Clear Register. Further, interrupts will not be reported to the carrier board unless control of Interrupt Request Line 0 has been configured via the Interrupt Enable Register.

**Event Polarity Control Register**

| BIT | WRITE "1" (NEGATIVE) | WRITE "0" (POSITIVE) |
|---|---|---|
| 0 | Negative Events on Port 0 IN00 through IN03 | Positive Events on Port 0 IN00 through IN03 |
| 1 | Negative Events on Port 0 IN04 through IN07 | Positive Events on Port 0 IN04 through IN07 |
| 2 | Negative Events on Port 1 IN08 through IN11 | Positive Events on Port 1 IN08 through IN11 |
| 3 | Negative Events on Port 1 IN12 through IN15 | Positive Events on Port 1 IN12 through IN15 |
| 4 | Negative Events on Port 2 IN16 through IN19 | Positive Events on Port 2 IN16 through IN19 |
| 5 | Negative Events on Port 2 IN20 through IN23 | Positive Events on Port 2 IN20 through IN23 |
| 6 | Negative Events on Port 3 IN24 through IN27 | Positive Events on Port 3 IN24 through IN27 |
| 7 | Negative Events on Port 3 IN28 through IN31 | Positive Events on Port 3 IN28 through IN31 |

**Bank Select Register**
**(Enhanced Mode Bank 1, Port 7, Write Only)**

Bits 6 & 7 of this register are used to select/monitor the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0-2) of eight registers may be addressed. Bank 0 is similar to the Standard Mode bank of registers. Bank 1 allows the 32 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of the event inputs. Bits 0-5 of this register are not used. Bits 7 and 6 select the bank as follows:

**Bank Select Register**

| BIT | Function |
|---|---|
| 0-5 | NOT USED |
| 6 | Bank Select Bit 0 |
| 7 | Bank Select Bit 1 |

**Bank Select Register (Write)**

| Bit 7 Bit 6 | BANK OF REGISTERS |
|---|---|
| 00 | Bank 0 - Read Inputs |
| 01 | Bank 1 - Event Status/Clear |
| 10 | Bank 2 - Event Debounce Control, Clock, & Duration |
| 11 | INVALID - DO NOT WRITE |

**Bank Select Status Register 1**
**(Enhanced Mode Bank 1, Port 7, Read Only)**

Bits 0-5 of this register are not used. Bits 6 & 7 of this register are used to indicate the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0-2) of eight registers may be addressed. Bank 0 is similar to the Standard Mode bank of registers. Bank 1 allows the 32 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of the event inputs. Bits 7 and 6 of this register select the bank as follows:

**Bank Selected Status Register (Read)**

| Bit 7 Bit 6 | BANK OF REGISTERS |
|---|---|
| 00 | Bank 0 - Read Inputs |
| 01 | Bank 1 - Event Status/Clear |
| 10 | Bank 2 - Event Debounce Control, Clock, & Duration |
| 11 | INVALID - DO NOT WRITE |

**BANK 2 REGISTERS**

**Debounce Control Register**
**(Enhanced Mode Bank 2, Port 0, Read/Write)**

This register is used to control whether each individual port is to be passed through the debounce logic before being recognized by the circuitry. A "0" disables the debounce logic, and a "1" enables the debounce logic. Debounce applies to both inputs and event sense inputs, and only in Enhanced Mode.

Furthermore after enabling the debounce circuitry, wait at least three times the programmed debounce duration prior to reading the input ports or event signals to insure valid data.

**Debounce Control Register**

| BIT | DEBOUNCE CONTROL |
|---|---|
| 0 | Port 0 (IN00-IN07) |
| 1 | Port 1 (IN08-IN15) |
| 2 | Port 2 (IN16-IN23) |
| 3 | Port 3 (IN24-IN31) |
| 4-7 | NOT USED |

| "0" | "1" |
|---|---|
| Disable | Enable |

**Debounce Duration Register 0**
**(Enhanced Mode Bank 2, Port 1, Read/Write)**

This register controls the duration of debounce on each input. Register 0 controls debounce for ports 0-3. The 8MHz IP system clock has the debounce times shown below. Note that this time applies to the FPGA input and does not include the opto-coupler time delay.

**Debounce Duration Register 0:**

| BIT | DEBOUNCE CONTROL |
|---|---|
| 0 | Port 0 Debounce Value Bit 0 |
| 1 | Port 0 Debounce Value Bit 1 |
| 2 | Port 1 Debounce Value Bit 0 |
| 3 | Port 1 Debounce Value Bit 1 |
| 4 | Port 2 Debounce Value Bit 0 |
| 5 | Port 2 Debounce Value Bit 1 |
| 6 | Port 3 Debounce Value Bit 0 |
| 7 | Port 3 Debounce Value Bit 1 |

**Duration (8MHz):**

| Bit 1,0 | Time |
|---|---|
| 00 | 4us |
| 01 | 64us |
| 10 | 1ms |
| 11 | 8ms |

This register is cleared following a reset.

**Debounce Clock Select Register**
**(Enhanced Mode Bank 2, Port 3, Write Only)**

On the original IP440, this register was used to select the 8MHz IP clock for debounce. The IP440A always uses the 8MHz clock for debounce and this register is only provided to facilitate backwards compatibility with the IP440. This register is cleared following a reset.

**Bank Select (Write) & Status (Read) Register 2**
**(Enhanced Mode Bank 2, Port 7, Read and Write)**

Bits 0-5 of this register are not used. Bits 6 & 7 of this register are used to indicate (read) or select (write) the bank of registers to be addressed. In Enhanced Mode, three banks (banks 0, 1, & 2) of eight registers may be addressed. Bank 0 registers are similar to the Standard Mode bank of registers. Bank 1 allows the 32 event inputs to be monitored and controlled. Bank 2 registers control the debounce circuitry of the event inputs. Bits 7 and 6 select/indicate the bank as follows:

**Bank Select (Write) & Status (Read) Register**

| Bit 7 Bit 6 | BANK OF REGISTERS |
|---|---|
| 00 | Bank 0 - Read Input Signals |
| 01 | Bank 1 - Event Status/Clear |
| 10 | Bank 2 - Event Debounce Control, Clock, & Duration |
| 11 | INVALID - DO NOT WRITE |

**INDEPENDENT FIXED FUNCTION CONTROL REGISTERS**

**Interrupt Enable & Software Reset Register**
**(Read/Write, Base + 1EH)**

Bit 0 of this register specifies if the internal event sense interrupts are to be reported to the carrier or not (i.e. whether they drive INTREQ0 or not). This bit defaults to 0 (interrupt request disabled) and event interrupts are only flagged internally. That is, you would have to poll the Event Status Register to determine if an interrupt had occurred, and the INTREQ0 line would not be driven. If bit 0 of this register is set to “1”, then interrupts will drive the INTREQ0 line and permit Interrupt Select Cycles (INTSEL) to occur. This bit is cleared following a system reset, but not a software reset.

Writing a 1 to the bit 1 position of this register will cause a software reset to occur (be sure to preserve the current state of bit 0 when conducting a software reset). This bit is not stored and merely acts as a trigger for software reset generation (this bit will always read back as 0). The effect of a software reset is similar to a carrier reset, except that it is not driven by the carrier. The Interrupt Vector Register and the Interrupt Enable Bit of this register are not cleared in response to a software reset. Bits 2-7 of this register are not used and will always read high (1’s).

**Interrupt Vector Register (Read/Write, Base + 2EH)**

This 8-bit read/write register is used to store the interrupt vector that will be served (read) during an interrupt select cycle. In response to an interrupt select cycle, the IP module will execute a read of this register. Interrupts are only generated for events while in the Enhanced Mode (see Interrupt Enable register). This register is cleared following a system reset, but not a software reset. Interrupts will not be reported to the carrier board unless control of the Interrupt Request Line 0 (IntReq0) has been enabled via the Interrupt Enable Register (IER).

**IP Identification PROM - (Read Only, 32 Odd-Byte Addresses)**

Each IP module contains an identification (ID) PROM that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID PROM. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP440A ID PROM does not contain any variable (e.g. unique calibration) information. ID PROM bytes are addressed using only the odd addresses in a 64 byte block (on the “Big Endian” VMEbus). Even addresses are used on the “Little Endian” PC bus. The IP440A ID PROM contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID PROM.

**Table 3.2: IP440A ID Space Identification (ID) PROM**

| Hex Offset From ID PROM Base Address | ASCII Character Equivalent | Numeric Value (Hex) | Field Description |
|---|---|---|---|
| 01 | I | 49 | All IP's have 'IPAC' |
| 03 | P | 50 | |
| 05 | A | 41 | |
| 07 | C | 43 | |
| 09 | | A3 | Acromag ID Code |
| 0B | | 10 | IP Model Code[1] |
| 0D | | 00 | Not Used (Rev) |
| 0F | | 00 | Reserved |
| 11 | | 00 | Not Used (Driver ID Low Byte) |
| 13 | | 00 | Not Used (Driver ID High Byte) |
| 15 | | 0C | Total Number of ID PROM Bytes |
| 17 | | 3B | CRC |
| 19 to 3F | | yy | Not Used |

**Notes (Table 3.2):**

1. The IP model number is represented by a two-digit code within the ID PROM (P440 model is represented by 10 Hex).
2. Execution of an ID PROM read requires 0 wait states.

**THE EFFECT OF RESET**

A power-up or bus-initiated software reset will place the module in the Standard Operating Mode (input only, no event sensing, no interrupts, and no debounce). Further, all event inputs are reset, set to positive events, and disabled following reset. A false input signal is ensured for inputs left floating (i.e. reads as 0). The Interrupt Enable Register (IER) and Interrupt Vector Register (IVR) are also cleared (except for IER generated software resets).

Another form of software reset (IER register initiated) acts similar to a carrier or power-up reset, except that it is not driven by the carrier. For the software reset, the Interrupt Vector Register and Interrupt Enable Register are not cleared. Reset in this manner has been provided for use when the interrupt vector and interrupt enable information must be preserved.

**Basic Input Operation**

Note that the input lines of this module are assembled in groups of eight. Each group of eight lines is referred to as a port. Ports 0-3 control and monitor input lines 0-31. Additionally, ports are grouped eight to a bank. There are four banks of ports used for controlling this module (Standard Mode, plus Enhanced Mode Banks 0, 1, and 2), plus 2 additional registers for enabling the interrupt request line, generating a software reset, and storing the interrupt vector.

Each port input line is bipolar and accepts both positive and negative input voltages in two ranges according to the model number. Individual input lines of a port share a common signal connection with each other. Separate commons are provided for each port to facilitate port-to-port isolation. A high signal is derived from the absolute value of the input voltage measured between the input line and the port common for the input ranges of 4-18V (IP440A-1 models), 16-40V (IP440A-2 models), and 38-60V (IP440A-3 models). Inputs are non-inverting and inputs left floating (not recommended) will register a low (false=0) input indication.

In both the Standard and Enhanced operating modes, each group of eight parallel input lines (a port) are isolated and gated to the data bus D0..D7 lines. A high input will read as “1” and all inputs include hysteresis and programmable debounce.

**Enhanced Operating Mode**

In the Enhanced Mode of operation, each port input may act as an event sensor and generate interrupts. Likewise, programmable debounce logic is also available. Event sensing is used to selectively sense high-to-low level, or low-to-high level transitions on the input lines at the range thresholds of 4V (“-1” units), 16V (“-2” units), and 38V (“-3” units). Event polarities may be defined as positive or negative for individual nibbles (groups of 4 input lines, or half ports). Interrupts may also be triggered by events. The optional debounce logic can act as a filter to “glitches” or transients present on received signals.

The Enhanced Mode is entered by writing four unique bytes to the Standard Mode Port 7 register, in consecutive order, without doing any reads or writes to any other port and with interrupts disabled. The data pattern to be written is 07H, 0DH, 06H, and 12H, and this must be written immediately after reset or power-up.

In Enhanced Mode, there are three groups (or banks) of eight registers or ports. The first group, bank 0, provides register functionality similar to Standard Mode (input level monitoring). The second group, bank 1, provides monitor and control of the event sense inputs. The third group, bank 2, is used to configure the debounce circuitry for each input while in the Enhanced Mode.

**Event Sensing**

The IP440A has edge-programmable event sense logic built-in for all 32 input lines, IN00 through IN31. Event sensing may be configured to generate an interrupt to the carrier, or to merely reflect the interrupt internally. Event sensing is enabled in Enhanced Mode only and inputs can be set to detect positive or negative events, on a nibble-by-nibble (group of 4 input lines) basis. The event sensing is enabled on an individual channel basis. You can combine event sensing with the built-in debounce control circuitry to obtain “glitch-free” edge detection of incoming signals.

To program events, determine which input lines are to have events enabled and which polarity is to be detected, high-to-low level transitions (negative) or low-to-high level transitions (positive). Set each half-port (nibble) to the desired polarity, and then enable each of the event inputs to be detected. Optionally, if interrupt requests are desired, load the interrupt vector register and enable the interrupt request line. Note that all event inputs are reset, set to positive events, and disabled after a power-up or software reset has occurred.

**Change-Of-State Detection**

Change-of-State signal detection requires that both a high-to-low and low-to-high signal transition be detected. On the IP440A, if change-of-state detection for an input signal is desired, two channels connected to the same input signal would be required--one sensing positive transitions, one sensing negative transitions. Since channel polarity is programmable on a nibble basis (group of four), the first nibble of a port could be configured for low-to-high transitions, the second nibble for high-to-low transitions. As such, up to 16 change-of-state detectors may be configured.

**Debounce Control**

Debounce is available in Enhanced Mode only. With debounce, an incoming signal must be stable for the entire debounce time before it is recognized as a valid input or event at the FPGA input. Note that the debounce time applies at the FPGA input and does not include the opto-coupler delay. You can combine debounce with event sensing to obtain “glitch-free” edge detection of incoming signals for all 32 channels. That is, the debounce circuitry will help filter out “glitches” or transients that can occur on received signals, for error-free edge detection and increased noise immunity.

The debounce circuitry uses the 8MHz carrier clock to derive the debounce times. With the 8MHz carrier clock, a debounce value of 4us, 64us, 1ms, or 8ms may be selected (see the Debounce Duration Register). As such, an incoming FPGA signal must be stable for the debounce time before it is recognized as a valid input or event.

Upon initialization of the debounce circuitry, be sure to delay by at least three times the programmed debounce time before reading any of the input ports or event signals to ensure that the input data is valid prior to being used by the software.

**Interrupt Generation**

This model provides control for generation of interrupts on positive or negative events, for all 32 channels. Interrupts are only generated in the Enhanced Mode for event channels when enabled via the Event Sense/Status Register. Writing 0 to the corresponding event sense bit in the Event Sense/Status Register will clear the event sense flip/flop. Successive interrupts will only occur if the event channel has been reset by writing a 1 to the corresponding event sense bit in the Event Sense/Status Register (after writing 0 to clear the event sense flip/flop). Interrupts may be reflected internally and reported by polling the module, or optionally reported to the carrier by enabling control of

the Interrupt Request line (Intreq0). Control of this line is initiated via Bit 0 of the Interrupt Enable Register (IER).

After pulling the IntReq0 line low and in response to an Interrupt Select cycle, the module will read (serve) the 8-bit interrupt vector stored in the Interrupt Vector Register. The IntReq0 line will be released as soon as the conditions generating the interrupt have been cleared or return to normal, and the event sense flip/flop has been cleared by writing 0 to the corresponding bit position of the Event Sense Status Register, or until the Interrupt Enable Register bit is cleared. Zero wait states are required to complete an interrupt select cycle.

Note that the state of the inputs (on/off) is determined by reading the corresponding port address while in bank 0 of the Enhanced Mode. However, the event sense status can only be read by reading the corresponding port address while in bank 1 of the Enhanced Mode. Remember, the event sense status is a flag that is raised when a specific positive or negative transition has occurred for a given input point, while the state refers to its current level.

Note that the Interrupt Enable Register and Interrupt Vector Register are cleared following a power-up or bus initiated software reset, but not a software reset initiated via writing a one to bit 1 of the Interrupt Enable Register. Keep this in mind when you wish to preserve the information in these two registers following a reset.

**Programming Example**

The following example outlines the steps necessary to configure the IP440A for Enhanced Mode operation, to setup event-generated interrupts, configure debounce, and read and write inputs. It is assumed that the module has been reset and no prior (non-default) configuration exists.

For this example, we will configure port 0 input points as a four-channel change-of-state detector. For change-of-state detection, both positive and negative polarities must be sensed and thus, two channels are required to detect a change-of-state on a single input signal. IN00-IN03 will be used to detect positive events (low-to-high transitions); IN04-IN07 will be used to detect negative events (high-to-low transitions). IN00 and IN04 will be tied to the first input signal, IN01 & IN05 to the second, IN02 & IN06 to the third, and IN03 & IN07 to the fourth. Any change-of-state detected on these input signal lines will cause an interrupt to be generated.

1. After power-up or reset, the module is always placed in the Standard Operating Mode. To switch to the Enhanced Mode, execute four consecutive write cycles to port 7 with the following data: 07H first, followed by 0DH, followed by 06H, then 12H.

   At this point, you are in Enhanced Mode bank 0. Port 7 would now be used to access register banks 1 & 2.

2. Write 80H to the port 7 address to select register bank 2 where debounce will be configured for our port 0 input channels.

   At this point, you are in Enhanced Mode Bank 2 where access to the debounce configuration registers is obtained.

3. We need to enable the 8MHz system clock to generate our debounce time. By default, the debounce clock is not enabled. Select the 8MHz system clock as the debounce clock by writing 01H to the port 3 address of this bank (Debounce Clock Select Register). T*his set is not required for the IP440A.*

4. The default debounce duration is 4us with the 8MHz clock enabled in step 3. This time applies to the FPGA input signal and does not include opto-coupler delay. Write 01H to the port 1 address of this bank to select a 64us debounce time (Debounce Duration Register 0). An incoming signal must be stable for the entire debounce time before it will be recognized as a valid input transition by the FPGA.

   Note that Debounce Duration Register 1 (port address 2) would be used to configure debounce durations for ports 4 & 5. Since ports 4 & 5 are not used by this model, Debounce Duration Register 1 has no effect.

5. Enable the debounce circuitry for port 0 inputs by setting bit 0 of the Debounce Control Register. Write 01H to the Port 0 address of this bank (Debounce Control Register).

   If the module had been configured earlier, you would first read this register to check the existing settings of debounce enable for the other ports of this module with the intent of preserving their configuration by adjusting the value written above.

6. Write 40H to the port 7 address to select register bank 1 where the event polarity requirements of our application will be configured.

   At this point, you are in Enhanced Mode Bank 1 where access to the event polarity/status registers is obtained.

7. For change-of-state detection, both positive and negative polarities must be sensed. As such, two channels are required to detect a change-of-state on a single input signal. For our example, IN00-IN03 will be used to detect positive events (low-to-high transitions); IN04-IN07 will be used to detect negative events (high-to-low transitions). Write 02H to the port 6 address to set IN00-IN03 to positive edge detection, and IN04-IN07 to negative edge detection.

   Note that this port address has a dual function depending on whether a read or write is being executed. As such, if the current polarity configuration for the other ports must be preserved, then it must be remembered since it cannot be read back.

8. To enable event sensing for the port 0 input points, write FFH to the Event Sense Status Register for port 0 input points at the port 0 address in this bank.

   Note that writing a 1 to a bit position enables the event sense detector, while writing a 0 clears the event sensed without enabling further event sensing.

9. Write 00H to the port 7 address to select register bank 0 where the port 0 input channels may be write-masked.

   Note that the port 7 address bank selection only operates from bits 6 & 7 of this register. Likewise, this register has a

dual function depending on whether a read or write is executed. As such, the polarity settings cannot be read back and must be remembered if they are to be preserved for successive writes.

At this point, you are in Enhanced Mode Bank 0 where access to the write-mask register is obtained.

10. For our example, port 0 input points are to be used for inputs only and writes to this port should be masked to prevent the possibility of data contention between the built-in output circuitry and the devices driving these inputs. Write 01H to the port 7 address to mask writes to port 0.

11. Read 01H from the port 7 address to verify bank 0 access (bits 6 & 7 are 0) and port 0 write masking (bit 0 is 1).

12. (OPTIONAL) Write your interrupt vector to the Interrupt Vector Register Address (Note that this register operates independent of the current bank since it does not reside at any of the bank addresses).

13. (OPTIONAL) Write 01H to the Interrupt Enable Register (IER) address location to enable IP control of the IP Interrupt Request 0 line (IntReq0).

    When a change-of-state is detected, IntReq0 will be pulled low (if the event sense detection circuitry has been enabled and IER bit 0=1). In response, the host will execute an Interrupt Select cycle and the contents of the Interrupt Vector Register will be provided. To enable further interrupts for an event that has already occurred at an input point, the Event Sense Status Register must be written with a 1 to re-enable event sensing for subsequent events (only after first writing 0 to the corresponding bit position to clear the event sense flip/flop).

    Note that the state of the inputs (on/off) can be determined by reading the corresponding port address while in bank 0 of the Enhanced Mode. However, the event sense status can only be determined by reading the corresponding port address while in bank 1 of the Enhanced Mode. Remember, the event sense status is a flag that is raised when a specific positive or negative transition has occurred for a given input point, while the state refers to its current level.

## 4.0 THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the Drawing 4502-046 as you review this material.

### IP440A OPERATION

The IP440A is built around a Field-Programmable Gate Array (FPGA) IC. The device provides the control interface necessary to operate the module, the IP identification space, all registers, and provides I/O interface and configuration functions. The FPGA monitors and controls the functions of the 32 digital inputs used by this model. It also provides debounce control and event sensing functions.

Individual opto-couplers for each channel provide isolation for the Model IP440A. Channels are isolated from each other in groups of 8. There are 8 channels to a group or port. Because the input lines of a single port share a common connection, the individual inputs are not isolated from each other within the same port. However, separate port commons are provided to facilitate port-to-port isolation.

Input opto-couplers of this device are bipolar and accept voltages in three ranges: ± (4-18V), ± (16-40V), and ± (38-60V), DC or AC peak. The opto-couplers connect to an FPGA that provides the I/O read/write functionality, interrupt handling, and debounce control.

### LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). P1 also provides +5V to power the module (the ±12V lines are not used). Not all of the IP logic P1 pin functions are used.

The FPGA installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O, Interrupt, and ID spaces and produces the chip selects, control signals, and timing required by the control registers, as well as, the acknowledgement signal required by the carrier board per the IP specification. It also stores the interrupt vector and controls whether event interrupts will drive the carrier board interrupt request line.

The ID PROM (read only) is implemented in the FPGA and provides the identification for the individual module per the IP specification. The ID PROM & configuration and control registers are all accessed through an 8-bit data bus interface to the carrier board.

### IP440 vs. IP440A

The IP440A is a fit, form, and functional replacement for the IP440. However due to changes in the hardware, there are some minor differences between the models. This includes a slight change in the threshold voltages and a change in the turn-on/turn-off time. Furthermore due to an increase in input hysteresis, the IP440A is specified with a typical turn-on and typical turn off voltage. See tables 4.1 through 4.3 for further details.

**Table 4.1: Threshold Voltage Comparison**

| | | On Threshold Voltage (V) | | | |
|---|---|---|---|---|---|
| **Board** | **Input Range** | **MIN[2]** | **On TYP[1,3]** | **Off Typ[1,4]** | **MAX[2]** |
| IP440-1 | ±4 to ±18 | ±1 | ±2 | ±2 | ±4 |
| IP440A-1 | ±4 to ±18 | ±1 | ±2 | ±1.75 | ±4 |
| | | | | | |
| IP440-2 | ±16 to ±40 | ±4 | ±6.4 | ±6.4 | ±16 |
| IP440A-2 | ±16 to ±40 | ±3 | ±7.0 | ±5.7 | ±16 |
| | | | | | |
| IP440-3 | ±38 to ±60 | ±8 | ±12.9 | ±12.9 | ±38 |
| IP440A-3 | ±38 to ±60 | ±6 | ±13.75 | ±11.2 | ±38 |

1. Typical defined at 25°C
2. Minimum and Maximum values are for the extended temperature range (IP440AE). See Section 6.0 of this manual, for further information.
3. On is defined as a low to high transition.
4. Off is defined as a high to low transition.

**Table 4.2: Input Hysteresis/Resistor Comparison**

| Board | Typical Input Hysteresis (V)[1] | Current Limiting Resistor (Ω) |
|---|---|---|
| IP440-1 | 0.08[2] | 2200 |
| IP440A-1 | 0.25 | 1620 |
| | | |
| IP440-2 | 0.08[2] | 12000 |
| IP440A-2 | 1.10 | 10000 |
| | | |
| IP440-3 | 0.08[2] | 27000 |
| IP440A-3 | 2.55 | 21500 |

1. Typical defined at 25°C
2. Typical values not specified for individual ranges. IP440 board minimum is 0.08V.

**Table 4.3: On-Time/Off-Time Comparison[1]**

| | On-Time Typ[2] | Off-Time Typ[3] |
|---|---|---|
| **IP440-X** | 15uS | 35uS |
| **IP440A-X** | 10uS | 15uS |

1. All values defined at 25°C
2. 0 Volts to Max Threshold Voltage
3. Max Threshold Voltage to 0 Volts

In addition further enhancements to the device include precision debounce (no longer contains -25% error) and a decrease in input capacitance. In addition, all IP read and write requests are acknowledged preventing a possible lock-up of the bus. Not-Used registers always read as zero unless otherwise noted in this manual. The original IP440 did not respond (Ack*) to Not Used Registers and any system response would be defined by the carrier (e.g. IP timeout).

The Debounce Clock Select Register (Bank 2: Port 3) no longer provides any functionality. The 8MHz IP clock is always selected for debounce. Note that this register is still provided to facilitate backwards compatibility by allowing applicable write cycles even though their use is not required.

One additional difference is the power-on initialization time for the IP440A has increased to 200ms maximum. The module will not respond to any signal for up to 200ms following power-up. For further details on the differences between the models please contact Acromag.

## 5.0 SERVICE AND REPAIR

### SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

### PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Verify that there are no blown fuses. Replacement of the carrier and/or IP with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

### WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the “Support” tab to access:

- Application Notes
- Frequently Asked Questions (FAQ’s)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the “Contact Us” tab.

Acromag’s application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

## 6.0 SPECIFICATIONS

**GENERAL SPECIFICATIONS**

Physical Configuration...............Single Industrial I/O Pack Module
Length.................................3.880 inches (98.5 mm).
Width..................................1.780 inches (45.2 mm).
Board Thickness..................0.062 inches (1.59 mm).
Max Component Height........0.314 inches (7.97 mm).
Connectors:
P1 & P2 ..............................IP logic (P1) & field (P2) interface connectors -.50-pin female receptacle header (AMP 173279-3 or equivalent).
Power:
+5 Volts (±5%)....................60mA, Typical; 150mA, Maximum.
±12 Volts (±5%) from P1......0mA Maximum (Not Used).

**ENVIRNOMENTAL**

Operating Temperature.............0 to +70°C. -40 to +85°C (E Versions)
Relative Humidity.......................5-95% non-condensing.
Storage Temperature.................-55°C to +150°C.
Isolation......................................Logic and field connections are optically isolated (see INPUT specifications). Individual ports are also isolated from each other. However, input lines of individual ports share a common connection and are not isolated from each other. Separate port commons are provided to facilitate port-to-port isolation. Logic and field lines are isolated from each other for voltages up to 250V DC (AC rms) on a continuous basis (unit will withstand a 1500V AC dielectric strength test for one minute without breakdown). This complies with test requirements outlined in ANSI/ISA-S82.01-1988 for the voltage rating specified.
Isolation Spacing........................Printed circuit board minimum isolation spacing is as follows: Port-to-Logic - 0.025” Minimum; Port-to-Port - 0.015” Minimum. These clearances apply to inner layer foil spacing (outer layer foil spacing is greater).
Radiated Field Immunity (RFI)....Complies with EN61000-4-3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with no digital upsets.
Conducted RF Immunity (CRFI)....Complies with EN61000-4-6 3V/rms, 150KHz to 80MHz) and European Norm EN50082-1 with no digital upsets.
Electromagnetic Interference Immunity (EMI)............................No digital upset under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Electrostatic Discharge Immunity (ESD)...........................Complies with EN61000-4-2 Level 3 (8KV enclosure port air discharge) and Level 2 (4KV enclosure port contact discharge) and European Norm EN50082-1.
Surge Immunity............................Not required for signal I/O per European Norm EN50082-1.
Electric Fast Transient Immunity EFT............................ Complies with EN61000-4-4 Level 2 (0.5KV at field I/O terminals) and European Norm EN50082-1.
Radiated Emissions................... Meets or exceeds European Norm EN50081-1 for class B equipment. Shielded cable with I/O connections in shielded enclosure are required to meet compliance.

**INPUTS**

Input Channel Configuration.......32 Optically isolated bipolar inputs. For DC or AC voltage applications within specified range limits.
Isolation Medium........................Photo-transistor opto-coupler, CEL PS2915-1 or equivalent. . UL & VDE rated for isolation voltages up 400V DC or AC rms (optocoupler only).
Bipolar Input Voltage Range.......AC or DC Volts peak, per model number: ±4V to ±18V (Model IP440A-1); ± 16V to ± 40V (Model IP440A-2); ± 38V to ± 60V (Model IP440A-3). Range is determined by value of the input current limiting resistors installed on the module.
Input Threshold..........................Refer to Table below. Typical values are at 25°C. The IP440A-1 model may be used to interface with open-drain TTL outputs when used with an appropriate pull-up to +5V (see Drawing 4502-048).

| IP440A Range | INPUT RANGE (DC or AC Peak) | Threshold Voltages (V) | | | |
|---|---|---|---|---|---|
| | | MIN | On TYP | Off TYP | MAX |
| -1 | ± 4V to ±18V | ±1V | ±2V | ±1.75V | ±4V |
| -2 | ±16V to ±40V | ±4V | ±7.0V | ±5.7V | ±16V |
| -3 | ±38V to ±60V | ±8V | ±13.75V | ±11.2V | ±38V |

| IP440AE Range | INPUT RANGE (DC or AC Peak) | Threshold Voltages (V) | | | |
|---|---|---|---|---|---|
| | | MIN | On TYP | Off TYP | MAX |
| -1 | ± 4V to ±18V | ±1V | ±2V | ±1.75V | ±4V |
| -2 | ±16V to ±40V | ±3V | ±7.0V | ±5.7V | ±16V |
| -3 | ±38V to ±60V | ±6V | ±13.75V | ±11.2V | ±38V |

Input Hysteresis......................... Refer to Table below.

| Board | Typical Input Hysteresis (V)[1] |
|---|---|
| IP440A-1 | 0.25V |
| IP440A-2 | 1.10V |
| IP440A-3 | 2.55V |

1. Typical values at 25°C.

Input Capacitance......................30pF Typical.

Turn-On Time............................Measured to point of positive event interrupt detection (IntReq0 pulled low) - 10us Typical (25°C) for a 0 to threshold input step. Time decreases as magnitude of the step is increased above threshold.

Turn-Off Time.............................Measured to the point of negative event interrupt detection (IntReq0 pulled low) - 15us Typical (25°C) for a threshold to 0V input step. Time increases as magnitude of the step value is increased from the threshold.

Input Debounce..........................Each input includes debounce circuitry with variable debounce times. Debounce times are programmable and derived from the 8MHz system clock, in combination with the debounce duration register value. Debounce times are applied at the FPGA input and do not include opto-coupler delay time. Debounce values of 4us, 64us, 1ms, and 8ms may be configured. Each debounce time has an error of up to ±375ns.

Interrupts...................................Each channel has configurable interrupts. They may be configured for high-to-low, low-to-high, and change-of-state (two channels required) event types.

Forward Voltage Drop................1.1V Typical, 1.3V Maximum (Diode) + I*R. Series input current-limiting resistors are 1.62K (IP440A-1), 10K (IP440A-2), or 21.5K (IP440A-3) and installed on board.

Input Current.............................Varies per model number and input signal voltage level. For Model IP440A-1, the current is computed by dividing the signal level minus 1.1V (TYP) , by its current limiting resistor (1620Ω for IP440A-1, 10000Ω for IP440A-2, and 21500Ω for IP440A-3).

**INDUSTRIAL I/O PACK COMPLIANCE**

Specification............................. This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4-1995 for 8MHz operation.

Electrical/Mechanical Interface…Single-Size IP Module.

I/O Space (IOSEL*).....................16-bit or 8-bit read/write of low byte.

ID Space (IDSEL*).......................8-bit read: Supports Type 1, 32 bytes per IP (Consecutive odd byte address).

Interrupt Space (INTSEL*)...........8-bit read of Interrupt Vector Register contents.

Memory Space (MEMSEL*)…….Not Used.

Power-Up Initialization Time........200mS Max. (During this time the IP module will ignore all signals.)

Access Times (8MHz Clock):
All Read/Write Cycles..........0 wait states (250ns cycle).

## APPENDIX

**CABLE: MODEL 5025-550-x (Non-Shielded)**
**MODEL 5025-551-x (Shielded)**

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The cables are available in 4, 7, or 10 feet lengths. Custom lengths (12 feet maximum) are available upon request. Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Application: Used to connect Model 5025-552 termination panel to carrier board 50-pin field connectors.
Length: Last field of part number designates length in feet (4, 7, or 10 feet standard). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg), packed.

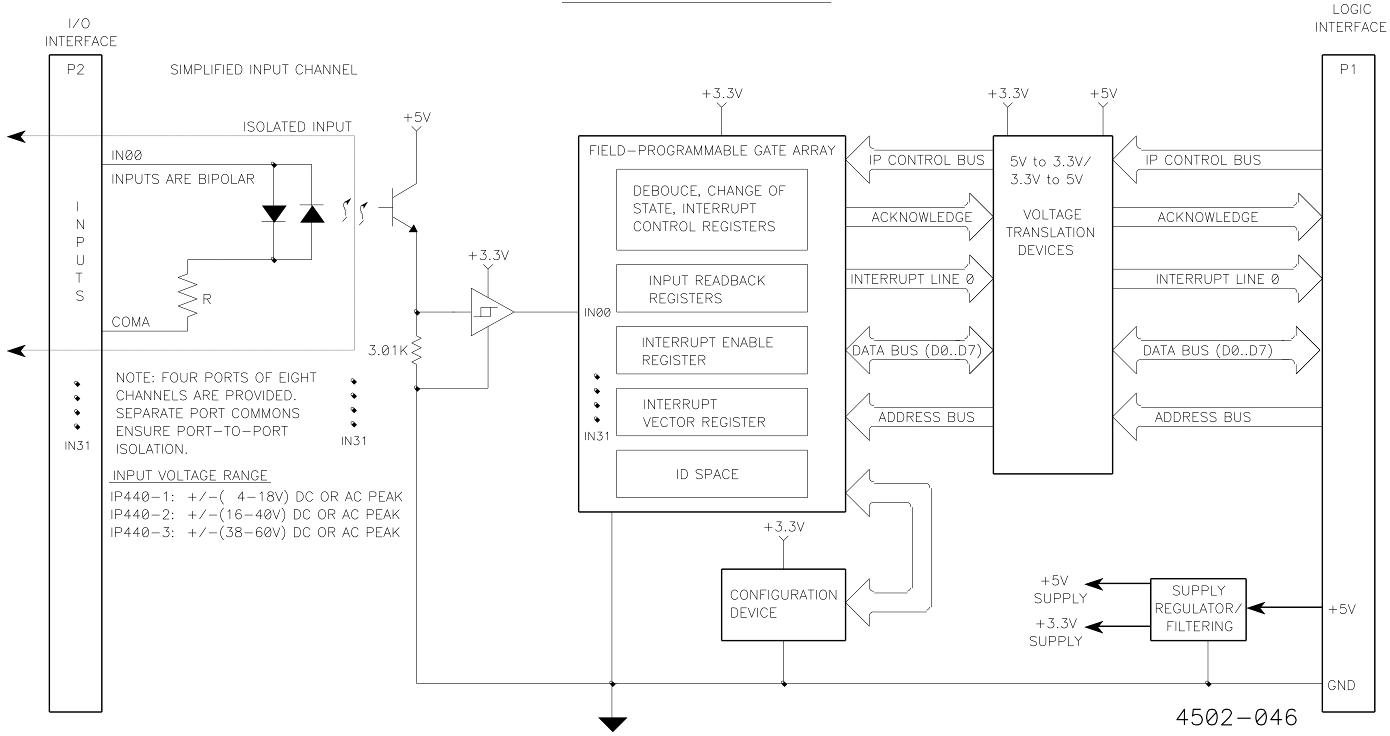
**TERMINATION PANEL: MODEL 5025-552**

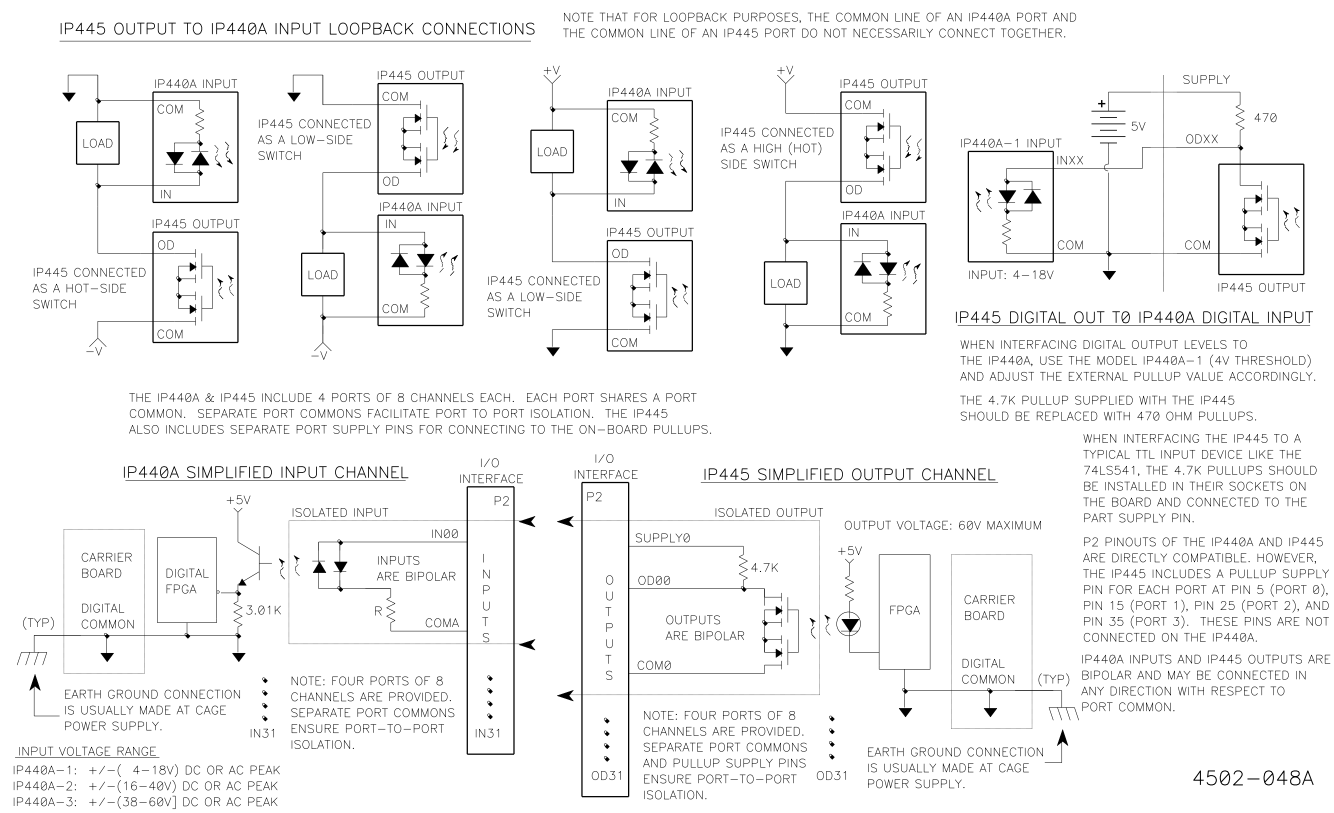
Type: Termination Panel For IP Carrier Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660/9668 or APC8620/21 non-intelligent carrier boards via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-E connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to Acromag non-intelligent carrier boards: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packed.

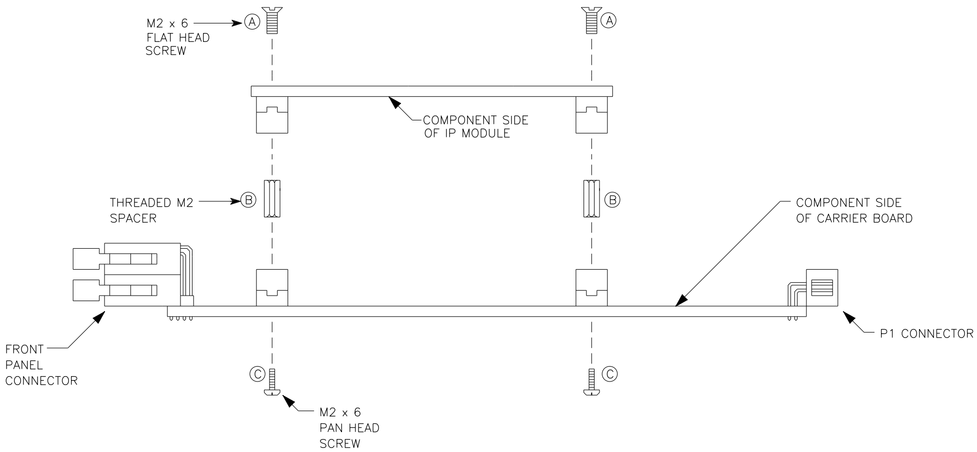
**TRANSITION MODULE: MODEL TRANS-GP**

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages, which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 50-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage, or to AVME9630/9660/9668 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X). Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40 to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packed.

## IP440A BLOCK DIAGRAM



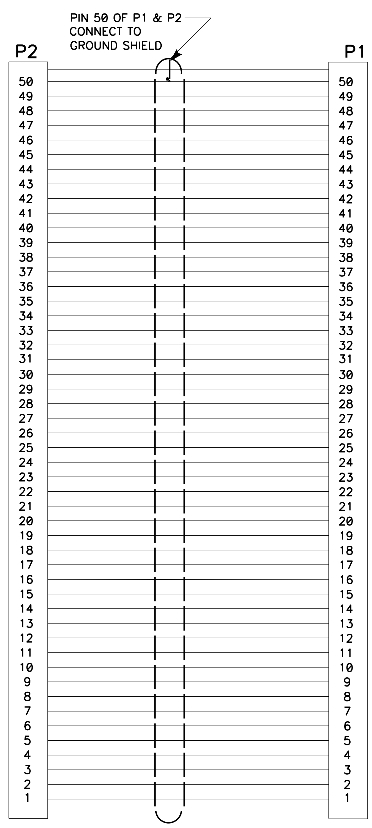



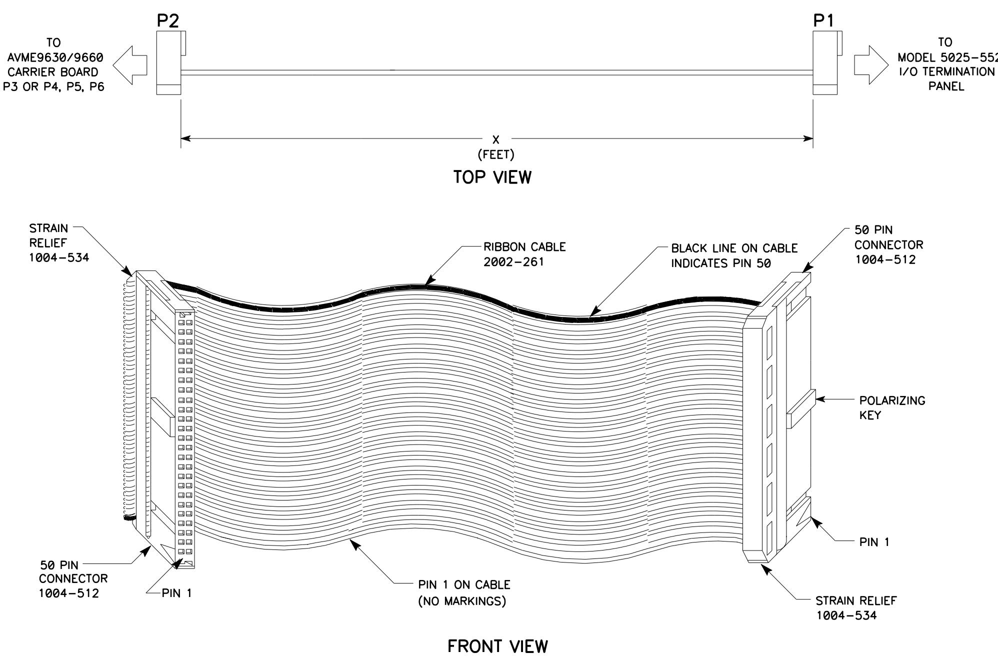



ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

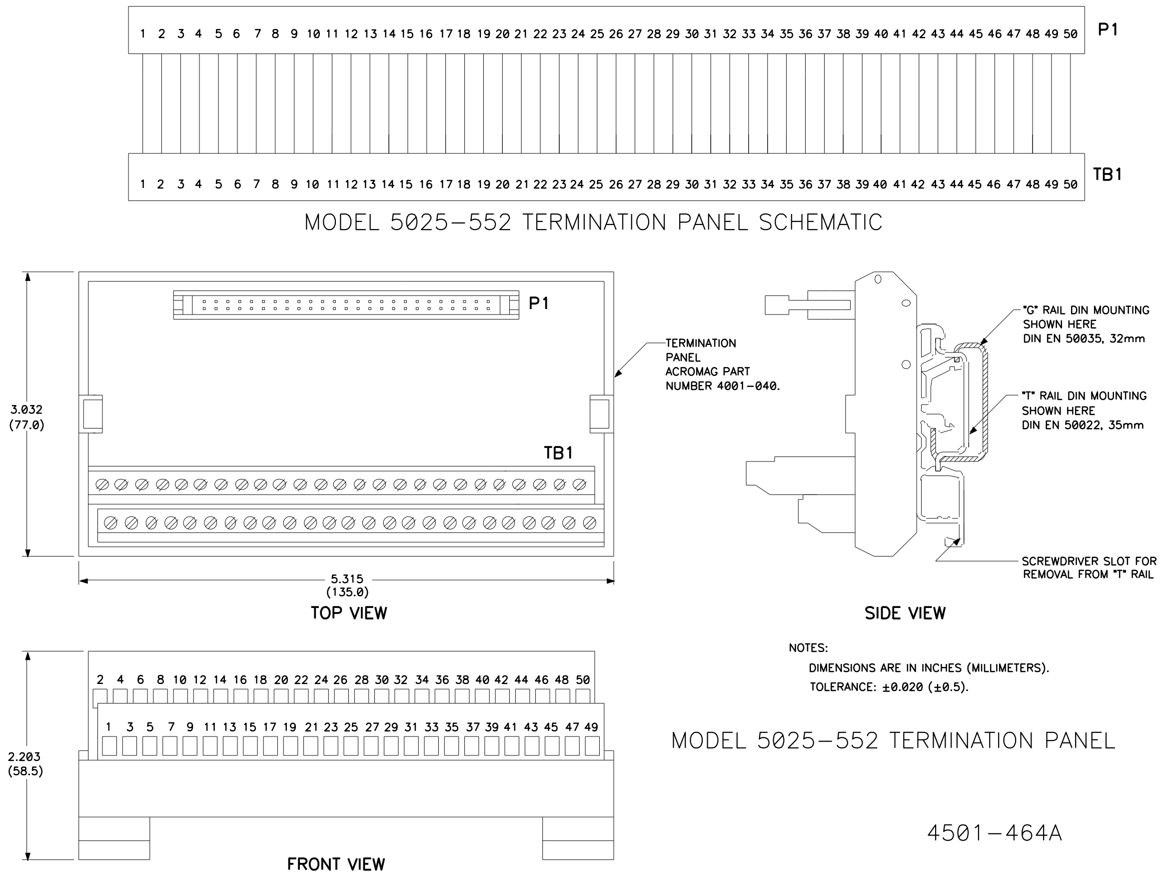
IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY 4501–434C



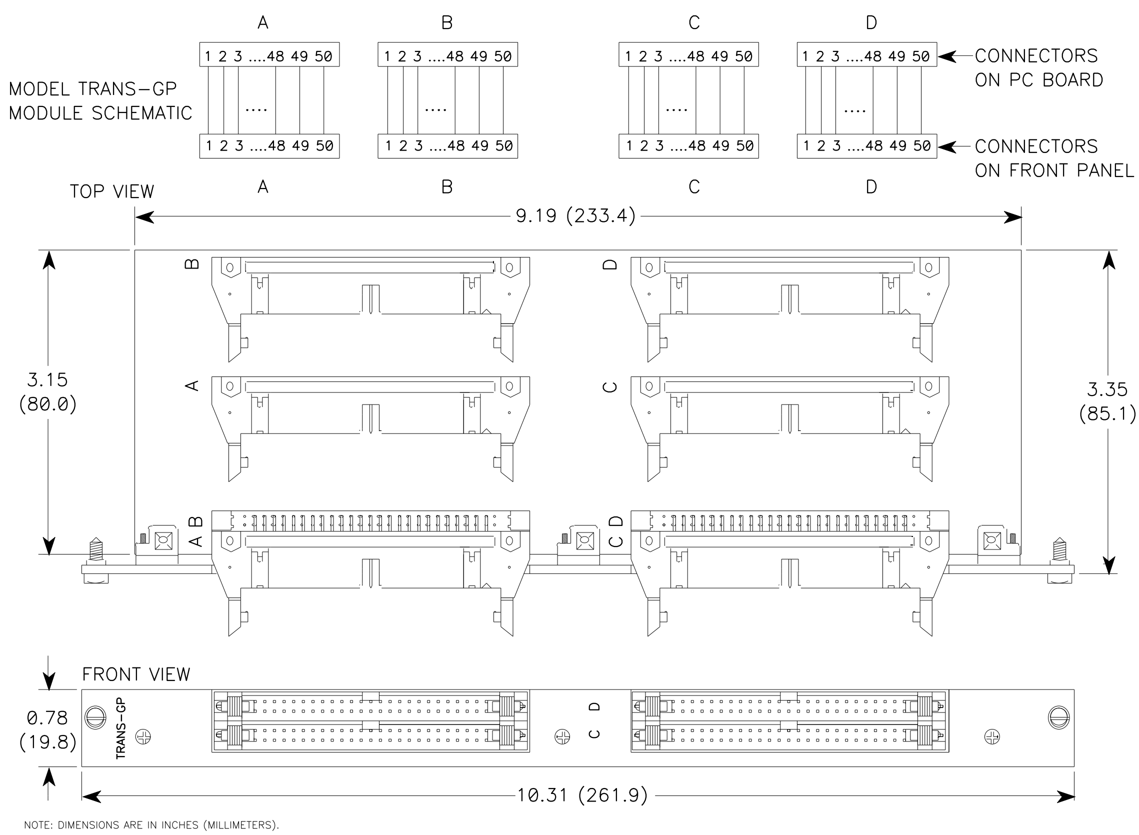

NOTE: SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS (XXXX-XXX).

MODEL 5025–551–x SCHEMATIC MODEL 5025–551–x SIGNAL CABLE, SHIELDED 4501–463A




MODEL 5025-552 TERMINATION PANEL

4501-464A




TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC 4501-465A